ESD Protection of RF Circuits in Standard CMOS Process

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Abstract: **The tradeoffs in the ESD protection device for RFCMOS circuits are described, and the characteristics of an SCR-based ESD structure are presented. The parasitic capacitance of the ESD structure is reduced to ~150fF. 3kV HBM and 750V CDM are achieved in a LNA working at 2.5GHz with NF<4dB, applicable for Bluetooth wireless transceiver.**

I. Introduction

Integration of RF transceiver circuits in core CMOS process is actively pursued [1] in an effort to increase functionality and reduce cost. Adequate Electro-Static Discharge (ESD) protection at high frequencies is a major challenge due to the speed degradation introduced by the parasitic capacitance of the ESD protection device [2, 3]. The conventional diode junction-based ESD protections are not adequate for deep-submicron CMOS due to high breakdown and holding voltages. Furthermore, the conventional I/O pad ESD protection cannot be used for RF devices due to large area and inherent parasitic capacitance.

In Ref.[2], the effect of ESD protection capacitance C_{ESD} was simulated for a 4GHz digital ring oscillator and an Op-Amp, but effects on RF characteristics were not reported. In [3], a diode-based ESD protection was implemented in a 0.35μm CMOS process for a 900 MHz LNA with off-chip input matching inductance. However, in both references, Charged Device Model (CDM) ESD stress were not reported. Furthermore, the intrinsic characteristics of the ESD protection devices and their effect on RF characteristics need more investigation.

In this work, firstly, ESD intrinsic characteristics of a SCR-based protection device with a trigger diode [4], which is illustrated in Fig.1, are compared with the conventional Gate-Grounded NMOS (GGNMOS) by Transmission Line Pulse (TLP) test. Next, the tradeoff between ESD strength and parasitic capacitance C_{ESD} is presented. Finally, the effects of the ESD protection device on RF gain, and noise figure of RF transistors and a 2.5GHz LNA are presented.

II. ESD Protection Devices Characteristics

The experimental evaluation was conducted on a standard 0.25μm, 4-level Al-Metal, logic-CMOS process on 10Ω.cm p-type bulk wafers. The process features twin-wells and shallow trench isolation.

The conventional GGNMOS and the lateral SCR-based [4] devices were evaluated for ESD protection. Both the structures were designed to have approximately the same current handling capability, i.e. same anode size. The *I-V* curves were measured by the TLP method, which approximates the situation for real ESD conditions. Fig.2 compares the TLP *I-V* characteristics for both devices. The first breakdown voltages are 8.5V and 9V for the SCR and the GGNMOS, respectively. For the SCR, the holding voltage (V_H) is ~4.0V which is enough to protect the 0.25μm transistors. The V_H is lower in the SCR device, which is beneficial for withstanding ESD stress. The superiority of the SCR results in a smaller protection device and less parasitic capacitance.

The main parameter determining the ESD strength is the anode size *Wa*. Fig.3 illustrates the measured Human Body Model (HBM) and CDM strength of the SCR device as a function of *Wa*. The ESD strength increases with *Wa*, nevertheless, the parasitic capacitance C_{ESD}, which is mainly determined by Nwell-Pwell junction capacitance, also increases. The equivalent circuit components (C_{ESD}, R_{ESD}) of the ESD protection structure, during normal operation, were extracted by S-parameters techniques in the 0.1~10GHz range. The relation between C_{ESD} and the SCR size is shown in Fig.4.

From the results in Figs. 3 and 4 it follows that the SCR-based protection device can achieve HBM>1kV and CDM>500V with a C_{ESD}~100fF.

III. The Effect on the RF Characteristics of the Transistor

The transition frequency f_T of the MOS transistor is reduced by the parasitic capacitance at the gate,

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$$f_T = \frac{g_m}{2\pi(C_g + C_{ESD})} = \frac{f_{Ti}}{1 + \frac{C_{ESD}}{C_g}} \quad (1).$$

Where C_g, g_m and f_{Ti} are the transistor's intrinsic gate capacitance, transconductance, and transition frequency, respectively. The noise factor is also degraded by the f_T reduction,

$$F_{min} \cong 1 + K\left(1 + \frac{C_{ESD}}{C_g}\right) \times \left(\frac{f}{f_{Ti}}\right) \times \sqrt{g_m(R_g + R_s)} \quad (2).$$

Where R_g and R_s are the gate resistance and source resistance, respectively. From these relations, it is clear that the degradation of RF characteristics depends on the ratio (C_{ESD}/C_g), and therefore it would become more significant for small size transistors. Figs. 5 and 6 show the measured transition frequency f_T and the minimum noise figure NFmin=10xlog(Fmin) at 2GHz of the NMOS transistors (W/L=300μm/0.24μm) without and with a *Wa*=100μm SCR-based ESD protection device connected between the input gate pad and the GND source pad. The noise figure is reduced by ΔNF~0.5dB by the effect of the ESD parasitic capacitance. For this structure (C_{ESD}/C_g) ~ 0.7 and the f_T and NFmin degradations are well explained by (1) and (2).

IV. ESD Protected Low Noise Amplifier (LNA)

In this section, the application of the lateral SCR-based ESD protection device to an RF LNA and the effect of the ESD size on the LNA characteristics are presented.

Based on the evaluation results of the unit SCR devices, a low-current consumption 2.5-GHz, NF<4dB LNA for short-range wireless transceiver applications (Bluetooth, WLAN), was designed. A schematic of the LNA is shown in Fig.7. The input transistor should be as large as possible to minimize the effect of ESD protection device capacitance. In this design, the transistors are W/L=300μm/0.24μm, which results in a total gate capacitance C_g~600fF, consequently, (C_{ESD}/C_g~1/4) for the *Wa*=25μm ESD protection device. For cost reduction, the matching inductors are implemented on chip, and feature the quality factor Q~5.

For ESD protection, (a) minimum size SCR were attached between the RF input pad and ground (P1), and (b) large size SCR's for bias and low-frequency pads. For evaluation, the LNA devices were assembled in QFP-48pin packages

Three designs of the basic LNA were fabricated with and without the input ESD protection. The nominal supply voltage and current are *Vdd*=2.5V and *Idd*=5.5mA. Fig.8 shows the measured gain (S_{21}) versus frequency of the three LNA's. Fig.9 shows the gain and noise figure NF as a function of the ESD device size at 2.5GHz. Due to the parasitic ESD effect, the gain and NF are slightly degraded by –0.02dB/μm and 0.01dB/μm, respectively, as the SCR size *Wa* increases. NF is still <4dB even for the 25μm size device.

Fig.10 shows the measured ESD HBM and CDM strengths for the LNA versus *Wa*. For the 25μm size device, HBM>3kV and CDM~750V are met. The layout area of this device is approximately 350μm^2.

V. Conclusion

The tradeoffs in the design of the ESD protection device for RFCMOS circuits were described. The degradation of the RF characteristics, by the ESD protection device capacitance C_{ESD}, depends on the ratio of C_{ESD} and input transistor gate capacitance. This ratio must be minimized. Using an SCR-based protection device, the parasitic capacitance of the ESD structure is reduced to ~150fF. 3kV HBM and 750V CDM are achieved in an LNA working at 2.5GHz demonstrating the feasibility of reliable RF ICs on standard CMOS process.

Acknowledgement

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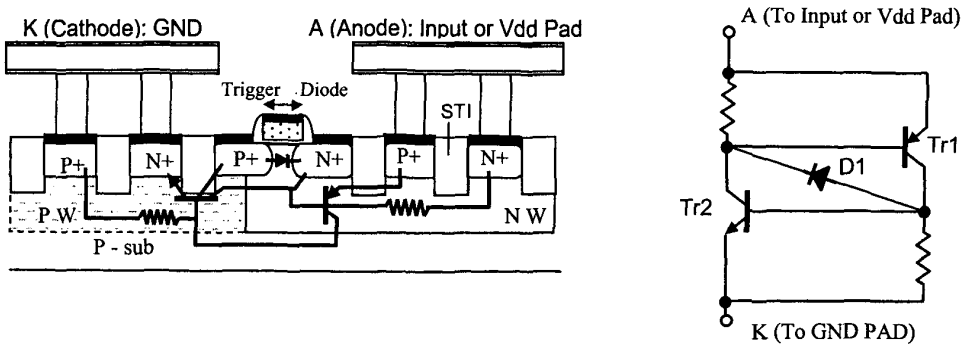

(a) (b)

Fig.1: Structure of the SCR: (a) cross-section, and (b) equivalent circuit.

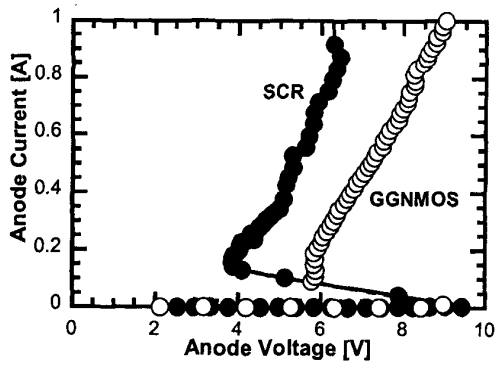

Fig. 2 Transmission-Line Pulsed I-V characteristics of the SCR (*Wa*=25um) compared with GGNMOS (*W*=30um).

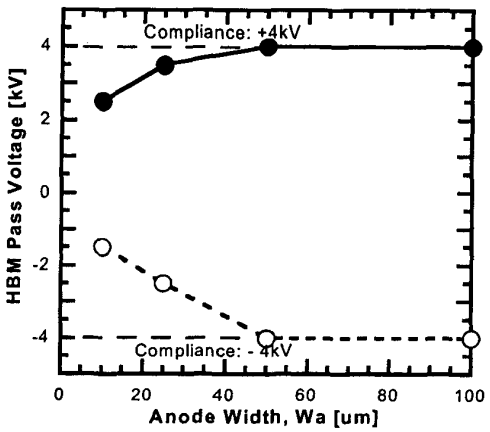

Fig. 3(a): SCR size effect on HBM pass voltage, measured in the unit SCR.

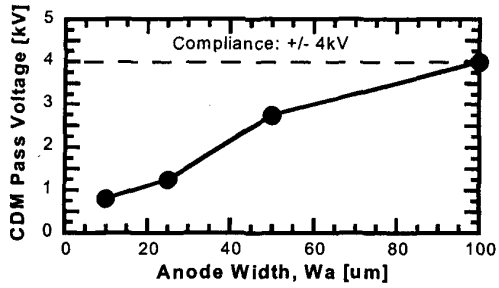

Fig. 3(b): SCR size effect on CDM pass voltage, measured in the unit SCR.

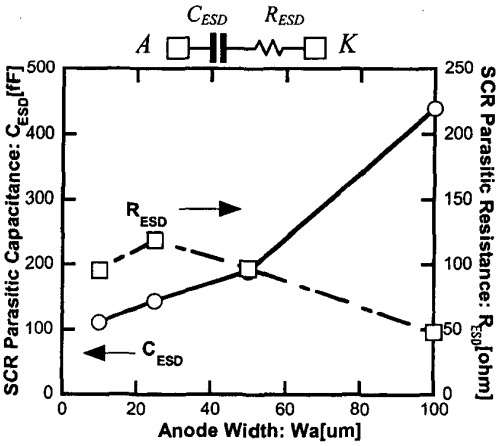

Fig. 4: SCR size effect on the equivalent circuit capacitance (C_{ESD}) and resistance (R_{ESD}) of ESD protection device as extracted from the S-parameter of the unit SCR in the 0.1-10GHz frequency range.

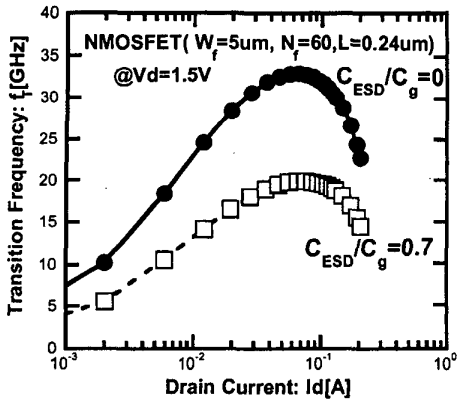

Fig.5: Measured effect of input ESD protection device capacitance (C_{ESD}) on the NMOSFET f_T-vs-*Id*.

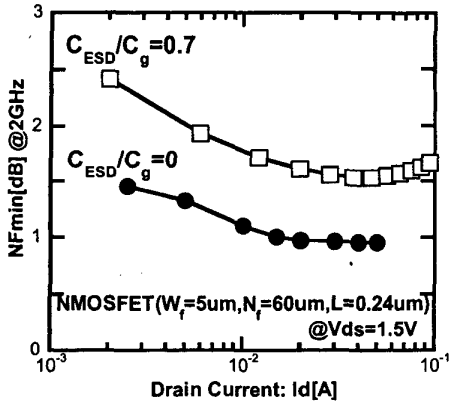

Fig.6: Measured effect of input ESD protection device capacitance (C_{ESD}) on the NMOSFET *NFmin*-vs-*Id*.

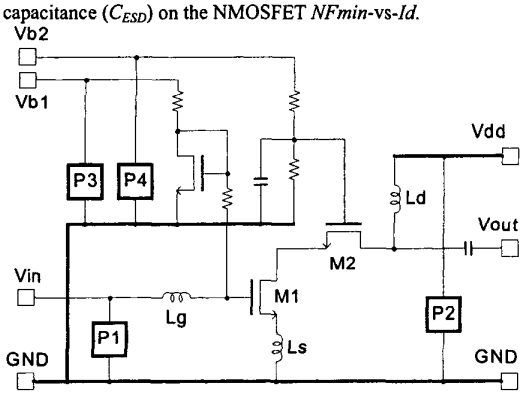

Fig. 7: Schematic of the ESD-protected LNA circuit. P1-P4 indicate the SCR-based ESD protection devices.

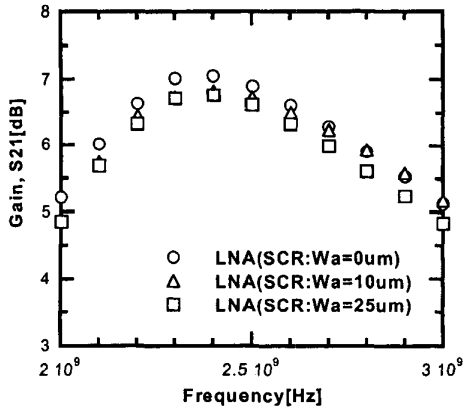

Fig. 8: Measured *S21*-frequency relationship of the LNA circuits with and without SCR's for input protection.

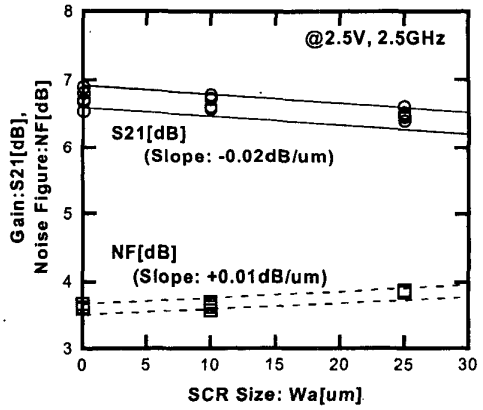

Fig. 9: Measured SCR Size effects on S21 and NF in the LNA. (Measurement: 5 points per each size)

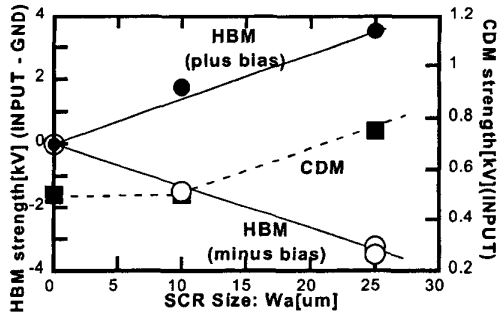

Fig. 10: Measured SCR Size effects on HBM and CDM strengths in the LNA.(Measurement: 5 points per each size)